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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/229,592	01/13/1999	BRIAN S. DOYLE	42390.P5578	5730

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EXAMINER	
BROCK II, PAUL E	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 03/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/229,592	DOYLE ET AL.	
	Examiner	Art Unit	
	Paul E Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19 and 28-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19 and 28-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on June 19, 2002. These drawings are acceptable.

Claim Rejections - 35 USC § 103

2. Claims 1 – 12, 16, 29, 30, and 32 – 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder et al. (USPAT 6063677, Rodder) in view of Sekine et al. (USPAT 5937300, Sekine).

Rodder discloses a method of forming a transistor in figures 3a – 5.

With regard to claim 1, Rodder discloses in figure 3a forming an alignment component (120 and 122) on a first portion of a substrate (102) of a semiconductor material. Rodder discloses in figure 3b and column 3, lines 5 – 40 depositing a metal layer (106) over the substrate and directly on a second portion of the substrate adjacent to the alignment component. Rodder discloses in column 3, lines 5 – 40 that the metal layer could also be a silicide layer formed by salicidation (salicide). Rodder discloses in column 3, lines 15 – 16 that the silicide regions are self aligned to the disposable gate. It is an inherent feature of silicide regions that are self-aligned to the disposable gate that they would extend up to the disposable gate and have inner surfaces which face one another. In figures 3e and 3f Rodder discloses removing the alignment

component. In figures 3e – 5 and column 5, lines 11 –26 Rodder discloses replacing the removed alignment component with a conductive gate (112). Rodder teaches in column 3, lines 27 – 32 that the silicide regions are formed by the salicide (self-aligned silicide regions) process. Rodder is silent to steps in the salicide process, however, the salicide process is well known in the art. Sekine teaches in figures 13b – 13d the salicide process. Sekine teaches in figure 13b and column 2, lines 1 – 30 depositing a metal layer (813) over a substrate (801) and a top and sides of an alignment component (805, 804 and 810) and directly on a second portion of the substrate adjacent to the alignment component. Sekine further teaches in figures 13b – 13c and column 2, lines 1 – 30 reacting the metal layer with the semiconductor material of the substrate to form two silicide regions (814) that are self aligned to the alignment component, the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the salicide process steps of Sekine that include lower and upper portions of silicide regions in the method of Rodder in order to use a well known and highly understood method of forming the silicide layers that will reduce interconnect resistance of the polysilicon lines. Because of the use of the salicide process by Rodder, as disclosed in column 3, lines 5 – 40, it can now be seen that Rodder discloses depositing a metal layer directly on a top and sides of the alignment component and directly on a region of the substrate adjacent to the alignment component, wherein previous to the depositing, the region of the substrate adjacent to the alignment component has not been doped differently than a region of the substrate, and subsequent to the depositing of the metal layer the region of the substrate

adjacent to the alignment component has not been doped. Further because Rodder discloses in column 3, lines 15 – 16 that the raised source and drain regions are self aligned to the disposable gate it is further obvious that the silicide regions of the combined method of Rodder and Sekine would produce silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate.

With regard to claims 2 – 4, Rodder discloses in columns 2 and 3, lines 59 – 67 and 1- 4 respectively that the alignment component includes silicon oxide which inherently posses the properties of being non-conductive, and in non-reactive with the metal layer when the metal layer is reacted with the semiconductor material of the substrate.

With regard to claims 5, 6 and 8, Rodder discloses in column 2, lines 11 – 17 that the alignment component is less than .10 microns wide. It is inherent that the alignment component has a thickness of between 1000Å and 2500Å. It is inherent that the metal layer is between 300Å and 400Å thick.

With regard to claim 7, Sekine discloses that the metal layer includes titanium in column 2, lines 4 – 6.

With regard to claim 9, Sekine discloses in figure 13c that the silicide regions have lower surfaces located lower than a lower surface of the alignment component.

With regard to claim 10, Rodder discloses in figures 3c – 5 a method wherein the alignment component is removed. In figure 3c Rodder discloses depositing a layer (114) over the silicide regions and the alignment component. In column 3, lines 46 – 49 Rodder discloses planarizing the layer at least until the alignment component is exposed. In figures 3e– 5 Rodder

discloses etching the alignment component at least until the substrate is exposed to leave an opening between the inner surfaces of the silicide regions to allow for formation of the gate (112).

With regard to claim 11, it would be obvious in the method of Rodder, Sekine and Ishida further comprising exposing the upper portions of the inner surfaces after the etching of the alignment component,. Because the alignment component and the upper portions of the inner surfaces are in contact as applied to claim 1, when the alignment component is removed, the upper portions of the inner surfaces would be exposed.

With regard to claim 12, Rodder discloses in columns 2 and 3, lines 59 – 67 and 1 – 52 respectively the alignment component and the layer are of different materials, one being of silicon oxide and the other being of silicon nitride.

With regard to claim 16, Rodder discloses in figure 4 forming doped regions (104) which extend from the silicide regions in underneath the gate.

Claims 29 and 32 are rejected similar to at least claims 4 and 9 – 12, respectively, with regard to Rodder, Sekine and Ishida, above. It is inherent that the silicide regions form a Schottky junction.

With regard to claim 30, it is further obvious in the method of Rodder, Sekine and Ishida that a portion of the metal layer above the alignment component is removed after the metal layer is reacted with the semiconductor material of the substrate.

With regard to claim 33, at least Sekine teaches in column 2, lines 40 – 44 wherein a substrate can be N-type or P-type. Therefore, it is further obvious in the method of Rodder and

Sekine wherein the first and second portions of the substrate are at least one of N-doped or P-doped.

With regard to claim 34, Rodder discloses a method of forming a transistor in figures 3a – 5. Rodder discloses in figure 3a forming an alignment component (120 and 122) on a first portion of a substrate (102) of a semiconductor material (the first portion being any portion is any region of the substrate between the alignment component and the bottom of the substrate). Rodder discloses in figure 3b and column 3, lines 5 – 40 depositing a metal layer (106) over the substrate and directly on a second portion of the substrate adjacent to the alignment component. Rodder discloses in column 3, lines 5 – 40 that the metal layer could also be a silicide layer formed by salicidation (salicide). Rodder discloses in column 3, lines 15 – 16 that the silicide regions are self aligned to the disposable gate. It is an inherent feature of silicide regions that are self-aligned to the disposable gate that they would extend up to the disposable gate and have inner surfaces which face one another. In figures 3e and 3f Rodder discloses removing the alignment component. In figures 3g, 3h, and 5, and column 5, lines 11 –26 Rodder discloses replacing the removed alignment component with a conductive gate (112), the first and second portions of the substrate being similarly doped (the substrate is inherently doped similarly throughout). Rodder teaches in column 3, lines 27 – 32 that the silicide regions are formed by the salicide (self-aligned silicide regions) process. Rodder is silent to steps in the salicide process, however, the salicide process is well known in the art. Sekine teaches in figures 13b – 13d the salicide process. Sekine teaches in figure 13b and column 2, lines 1 – 30 depositing a metal layer (813) over a substrate (801) and a top and sides of an alignment component (805, 804 and 810) and directly on a second portion of the substrate adjacent to the alignment component.

Sekine further teaches in figures 13b – 13c and column 2, lines 1 – 30 reacting the metal layer with the semiconductor material of the substrate to form two silicide regions (814) that are self aligned to the alignment component, the silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the salicide process steps of Sekine that include lower and upper portions of silicide regions in the method of Rodder in order to use a well known and highly understood method of forming the silicide layers that will reduce interconnect resistance of the polysilicon lines. Because of the use of the salicide process by Rodder, as disclosed in column 3, lines 5 – 40, it can now be seen that Rodder discloses depositing a metal layer directly on a top and sides of the alignment component and directly on a region of the substrate adjacent to the alignment component, wherein previous to the depositing, the region of the substrate adjacent to the alignment component has not been doped differently than a region of the substrate, and subsequent to the depositing of the metal layer the region of the substrate adjacent to the alignment component has not been doped. Further because Rodder discloses in column 3, lines 15 – 16 that the raised source and drain regions are self aligned to the disposable gate it is further obvious that the silicide regions of the combined method of Rodder and Sekine would produce silicide regions having inner surfaces which face one another, wherein an upper portion of each inner surface contacts the alignment component and a lower portion of each inner surface contacts the semiconductor material of the substrate.

With regard to claims 35 and 36, Rodder discloses in columns 2 and 3, lines 59 – 67 and 1- 4 respectively that the alignment component includes silicon oxide which inherently posses the properties of being non-conductive.

3. Claims 13 – 15 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder and Sekine as applied to claim 1 above, and further in view of Inumiya et al. (USPAT 6054355, Inumiya).

With regard to claims 13, Rodder discloses in figure 5, and column 4, lines 56 – 67 depositing a gate dielectric layer (110), and forming a gate electrode on the gate dielectric layer. Rodder does not disclose forming a dielectric layer that would be sufficient in Rodder and Sekine because the dielectric layer of Rodder would not insulate the entire upper portion of the inner surface of the silicide regions of Rodder and Sekine. Inumiya teaches in figure 10g depositing a gate dielectric layer (116) lining the inside of a groove (114) formed by the removal of an alignment feature, and forming a gate electrode (117) on the gate dielectric layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the gate dielectric layer of Inumiya in the method of Rodder and Sekine in order to form a gate insulating film and a gate electrode in a groove formed by the removal of an alignment feature.

With regard to claims 14 and 31, it is further obvious in the method of Rodder, Sekine, Masuoka and Inumiya that the gate dielectric could be less than 10Å thick. The gate dielectric could be less than 10Å thick in order to facilitate the gate requirements for the decreasing dimensions of semiconductor devices.

With regard to claim 15, Rodder discloses that the gate electrode includes a metal in column 4, lines 64 – 67.

4. Claims 17 – 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder, Sekine, and Inumiya as applied to claims 1 and 13 above, and further in view of Gardner et al. (USPAT 6051865, Gardner).

With regard to claims 17 and 18, Rodder, Sekine, and Inumiya do not disclose using a high K dielectric layer. Gardner teaches in columns 3 and 4, lines 24 – 40 and 24-36 respectively a gate dielectric layer of barium strontium titanate that has a dielectric constant of at least 100. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the low K dielectric material of Gardner in the method of Rodder, Sekine, and Inumiya in order to decrease the transistor threshold voltage as stated by Gardner in column 3, lines 26 – 33.

With regard to claim 19, Rodder, Sekine, , Inumiya and Gardner do not disclose using platinum as a gate electrode. It is well known in the art to form a gate electrode of platinum. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the platinum gate electrode in the process of forming a transistor of Rodder, Sekine, Inumiya and Gardner in order to use a low-resistivity conductor for the gate material.

5. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rodder and Sekine as applied to claim 1 above, and further in view of Wolf (Silicon Processing for the VLSI ERA, Vol. 2).

Rodder and Sekine obviously disclose that the silicide regions extend partially below the alignment component because that is a property of the silicide process as disclosed by the references. Rodder and Sekine do not disclose that the metal layer includes nickel. Wolf teaches on pages 146 a salicide formed from nickel. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the cobalt salicide of Wolf in the method of Rodder and Sekine in order to create a silicide that exhibits lower resistivities as taught by Wolf on page 146.

Response to Arguments

6. Applicant's arguments filed November 14, 2003 have been fully considered but they are not persuasive.

7. With regard to the applicant's argument that "Rodder does not teach or suggest reacting the metal layer with the semiconductor material of the substrate," it should be noted that Sekine is relied upon for this teaching. Based on the discussion of salicidation as presented in the rejection of claim 1 the claimed metal layer is reacted with the substrate. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore, the applicant's arguments are not persuasive, and the rejection is proper.

8. With regard to the applicant's argument that "Sekine does not teach or suggest reacting the metal layer with the semiconductor material of the substrate," it should be noted that Sekine clearly teaches this feature in figures 13a – 13d and the supporting sections of the written description in column 1, lines 32 – column 2, line 50. All of applicant's arguments are directed towards Sekine's embodiments shown in figures 1a – 1d and 2a – 2d, the rejection uses the embodiment of Sekine shown in figures 13a – 13d. As described in the above rejection, the portions 804, 805, and 810 make up the alignment component in Sekine. Sekine is not used to teach, "removing the alignment component." Further, Sekine is only used to show the well-known technique of salicidation to form salicide regions. Applicant does not suggest any reason why the combination of Rodder and Sekine fails. Therefore, applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (571) 272-2723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1164. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II

Tom Thomas